

1/10

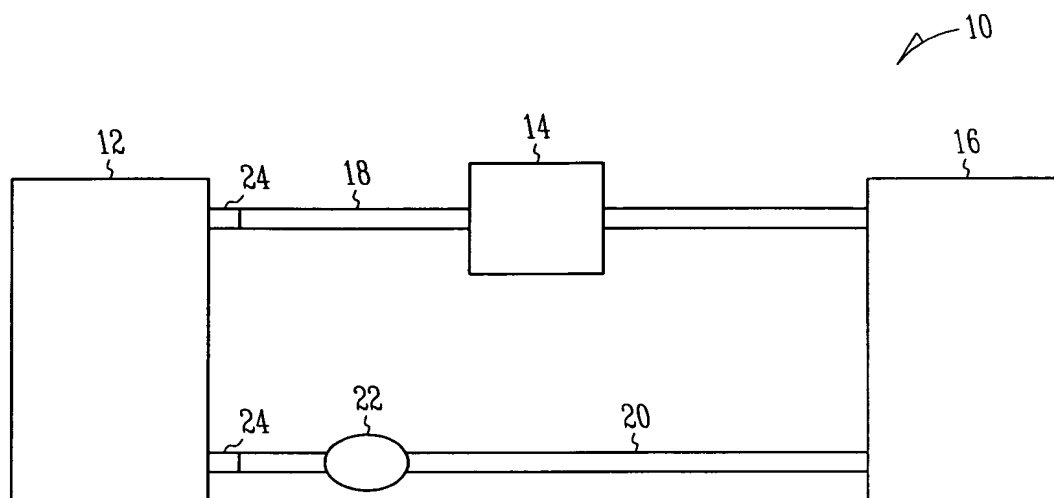


FIG. 1

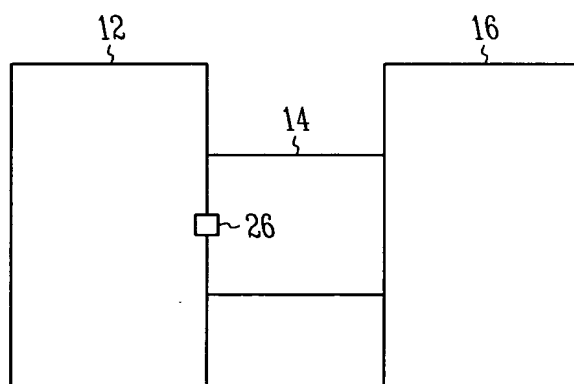


FIG. 2

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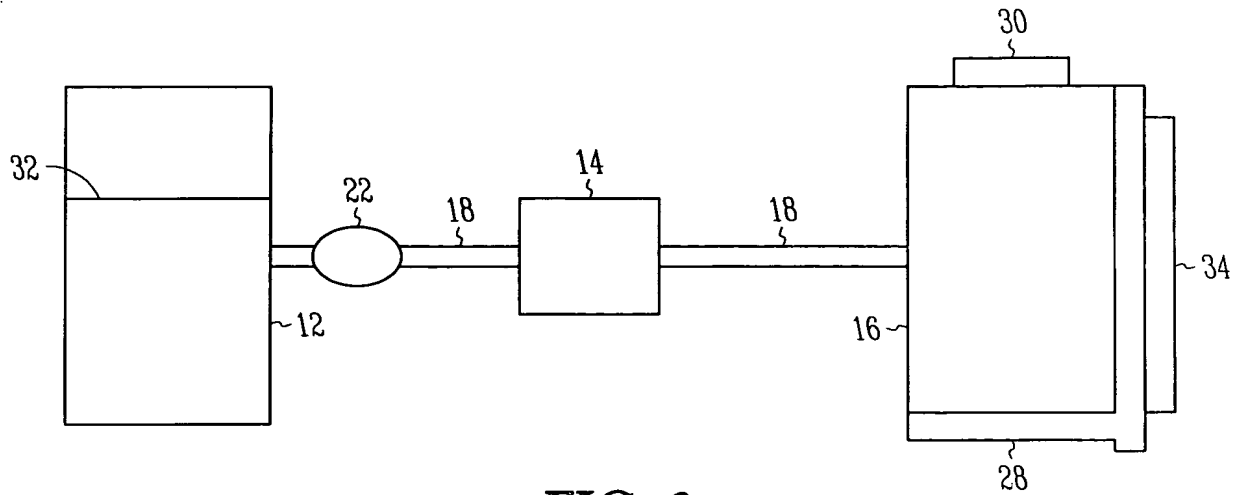


FIG. 3

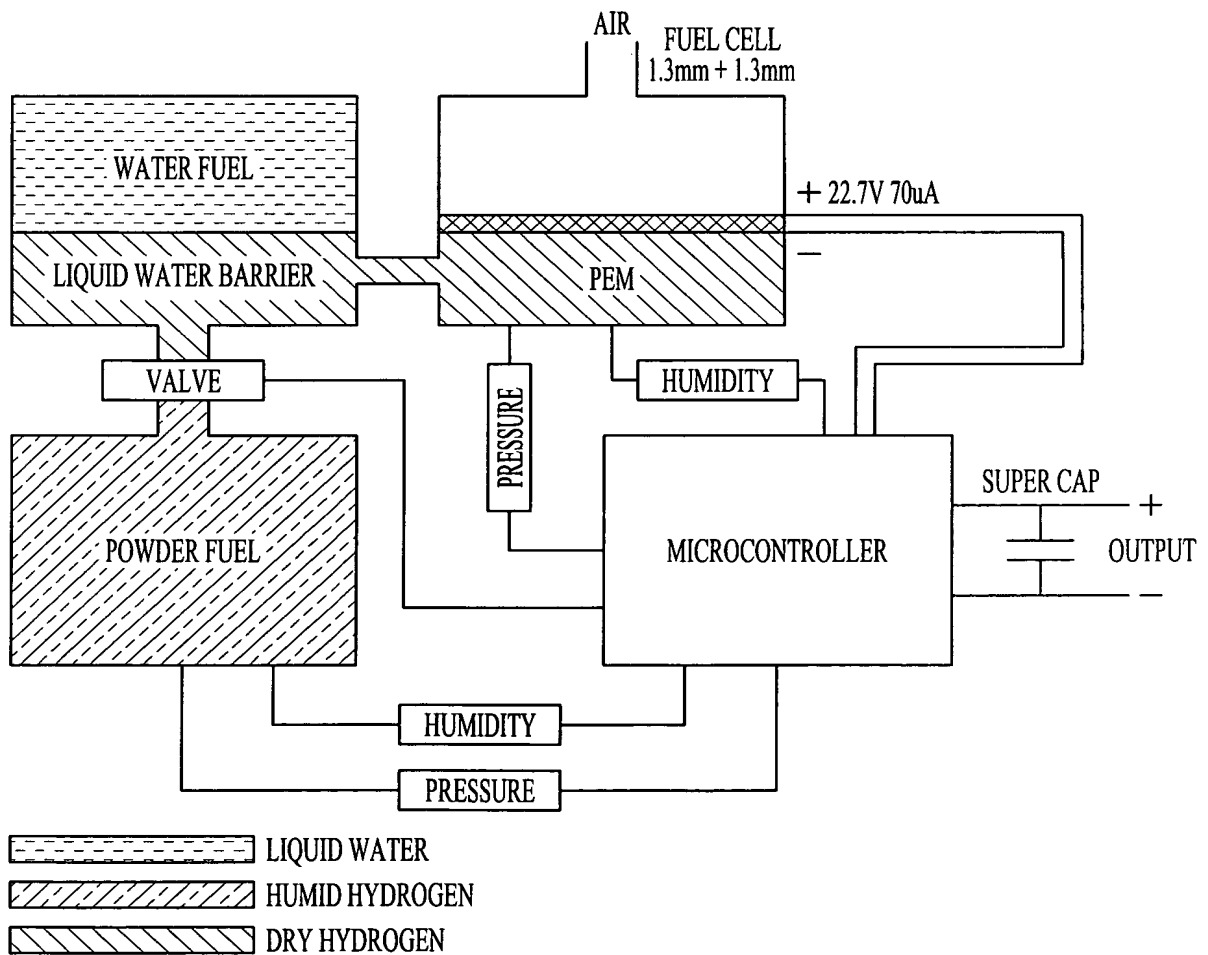


FIG. 4

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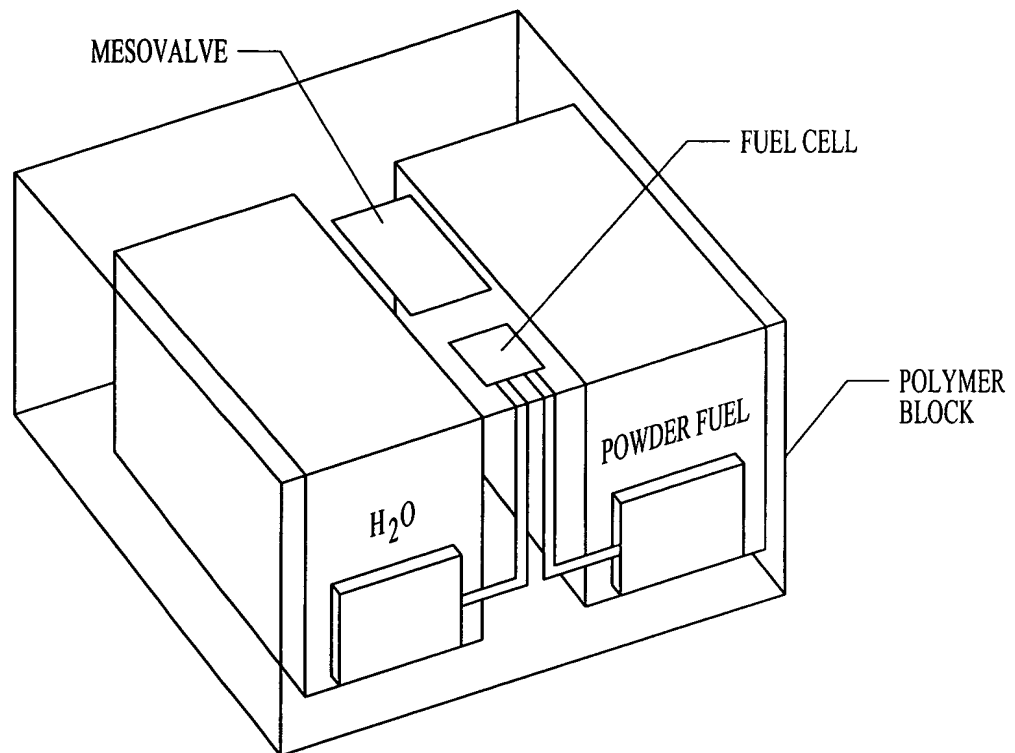


FIG. 5

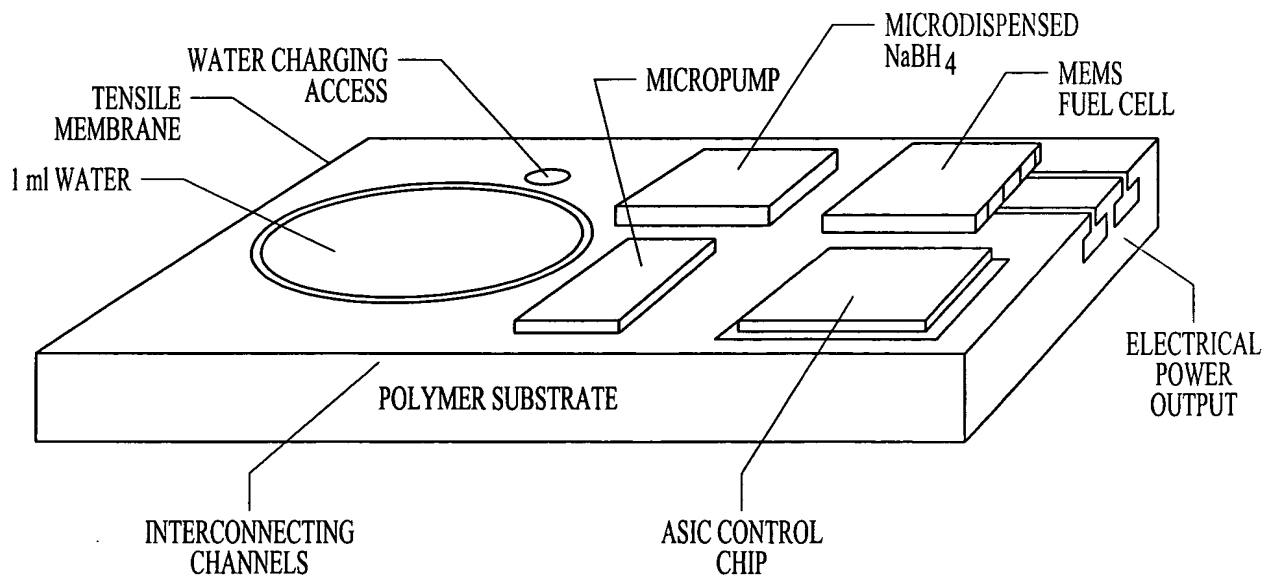


FIG. 6

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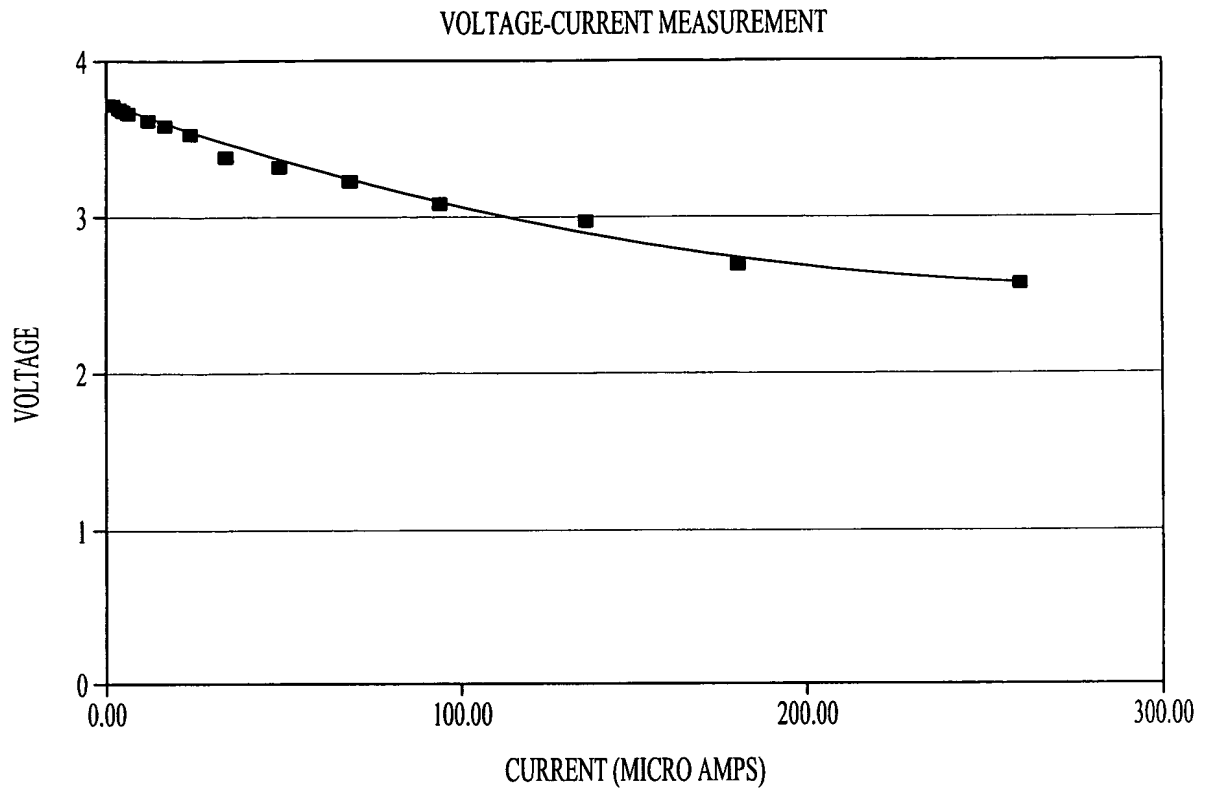


FIG. 7

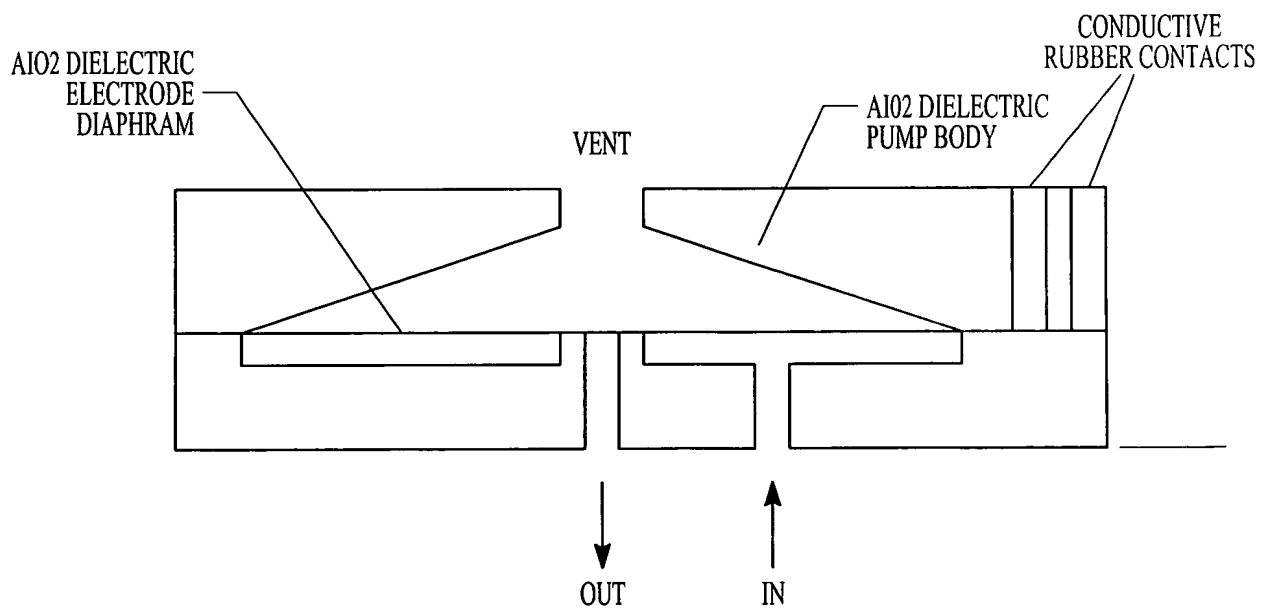


FIG. 8

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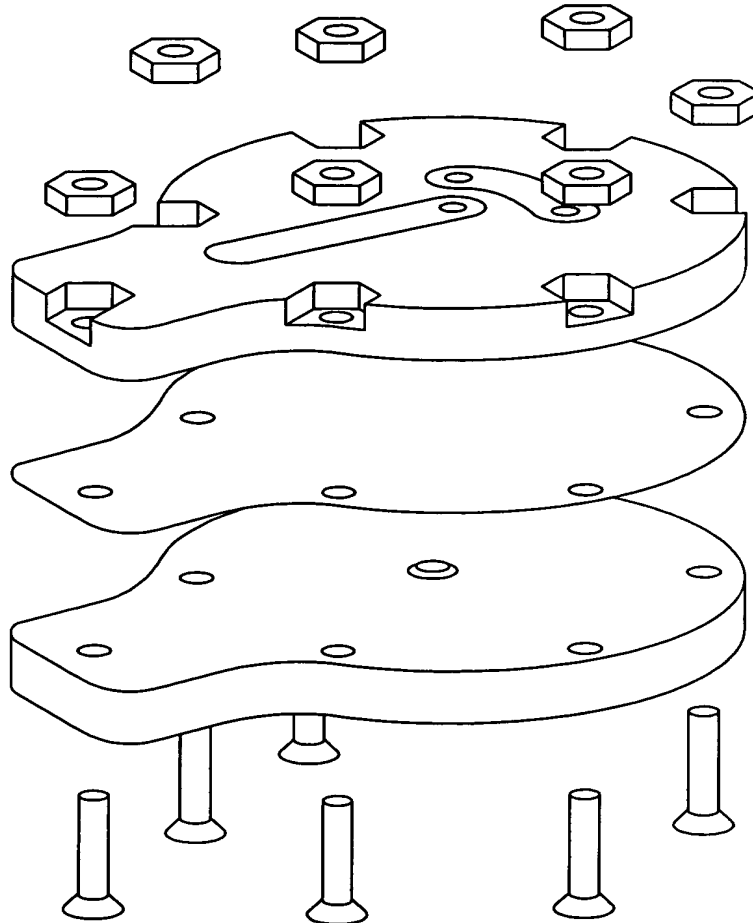


FIG. 9

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DOUBLE POLISHED Si WAFER WITH THERMAL OXIDE AND LPCVD NITRIDE SUITABLE
FOR CREATING THROUGH THE WAFER ETCH HOLES



FIG. 10A

STRIP OFF NITRIDE AND OXIDE FROM FRONT OF WAFER, GROW THIN THERMAL
OXIDE AND BRIDGE DIELECTRIC (NITRIDE)



FIG. 10B

DEPOSIT AND PATTERN LOWER ELECTRODE, SUCH AS TiW/Au OR Cr/Au



FIG. 10C

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DEPOSIT AND PATTERN LOWER ELECTRODE, SUCH AS TiW/Au OR Cr/Au

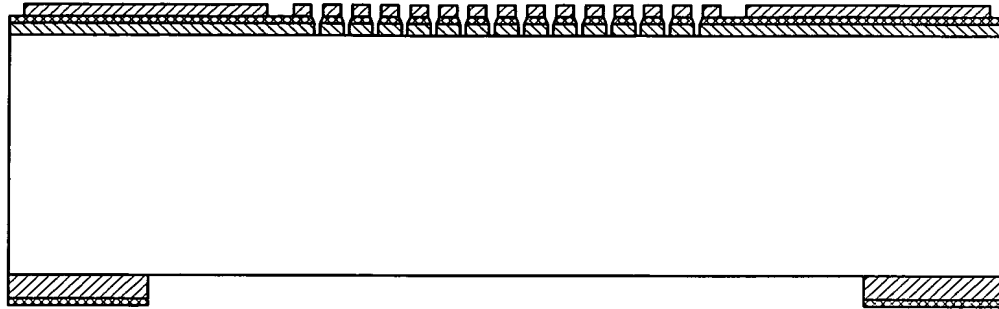


FIG. 10D

ETCH FROM BACKSIDE TO RELEASE DIAPHRAGMS



FIG. 10E

APPLY CATALYTIC PASTE BY "DOCTOR BLADING"

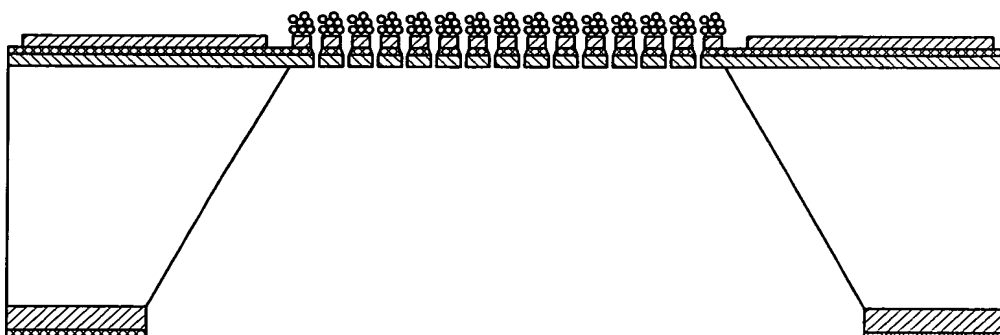


FIG. 10F

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APPLY PEM LAYER SUCH AS BY SPINNING

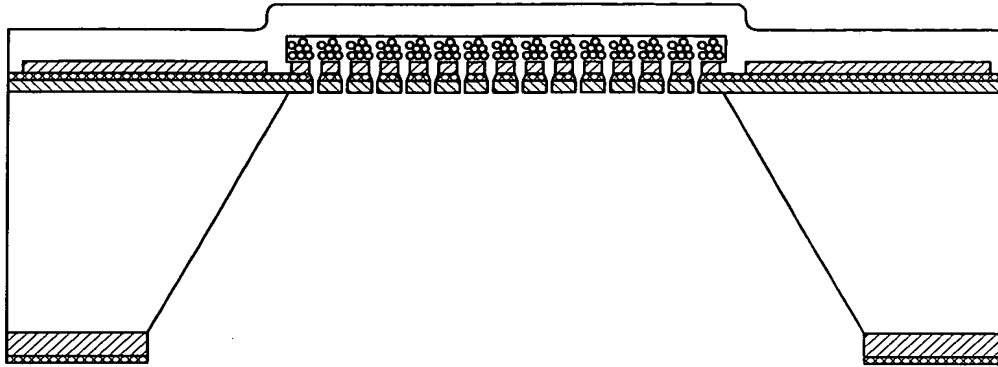


FIG. 10G

PATTERN PEM LAYER

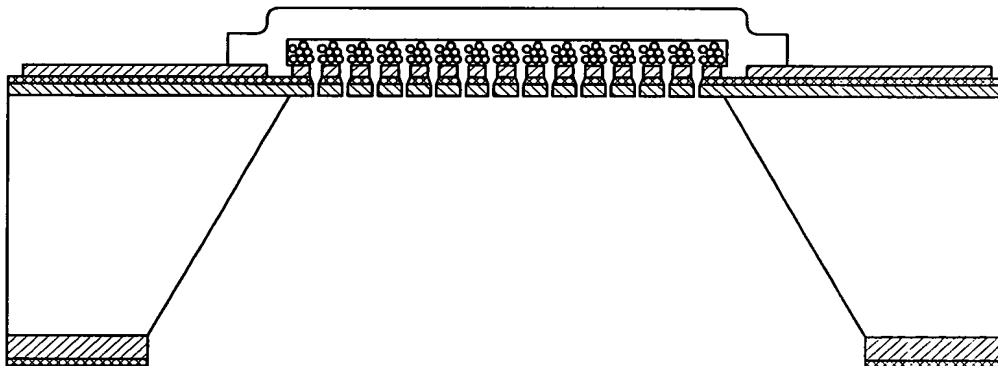


FIG. 10H

APPLY AND PATTERN UPPER ELECTRODE

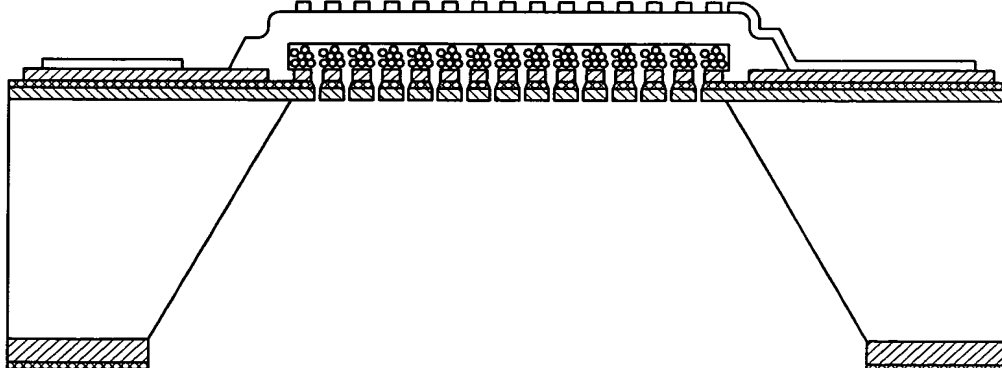


FIG. 10I

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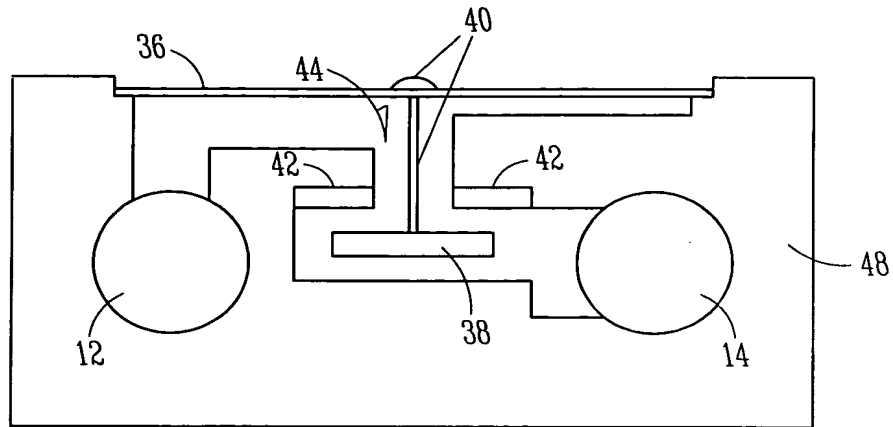


FIG. 11

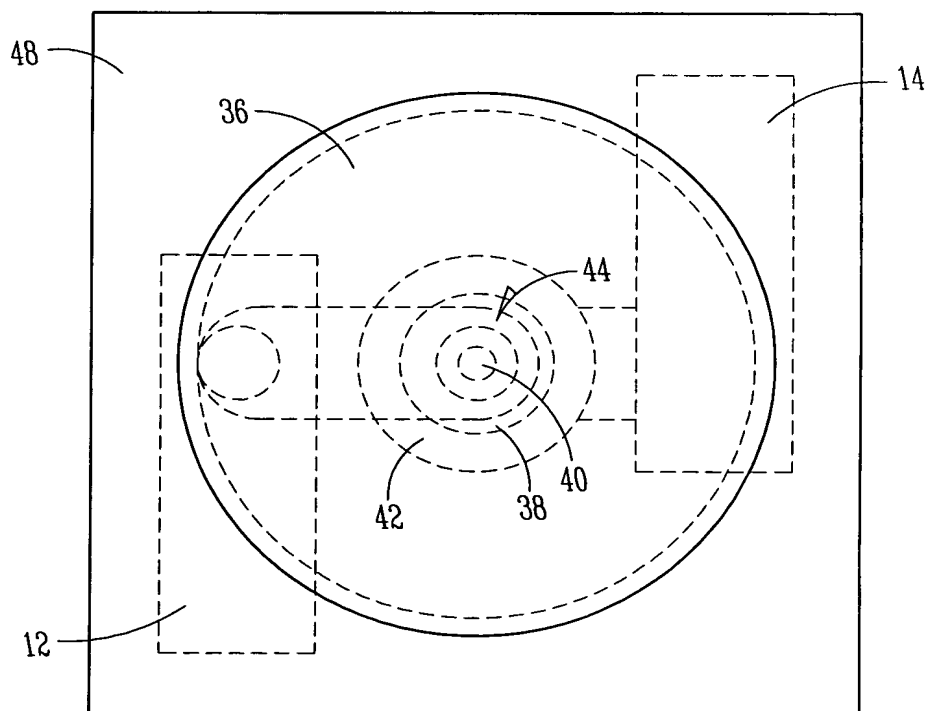


FIG. 12

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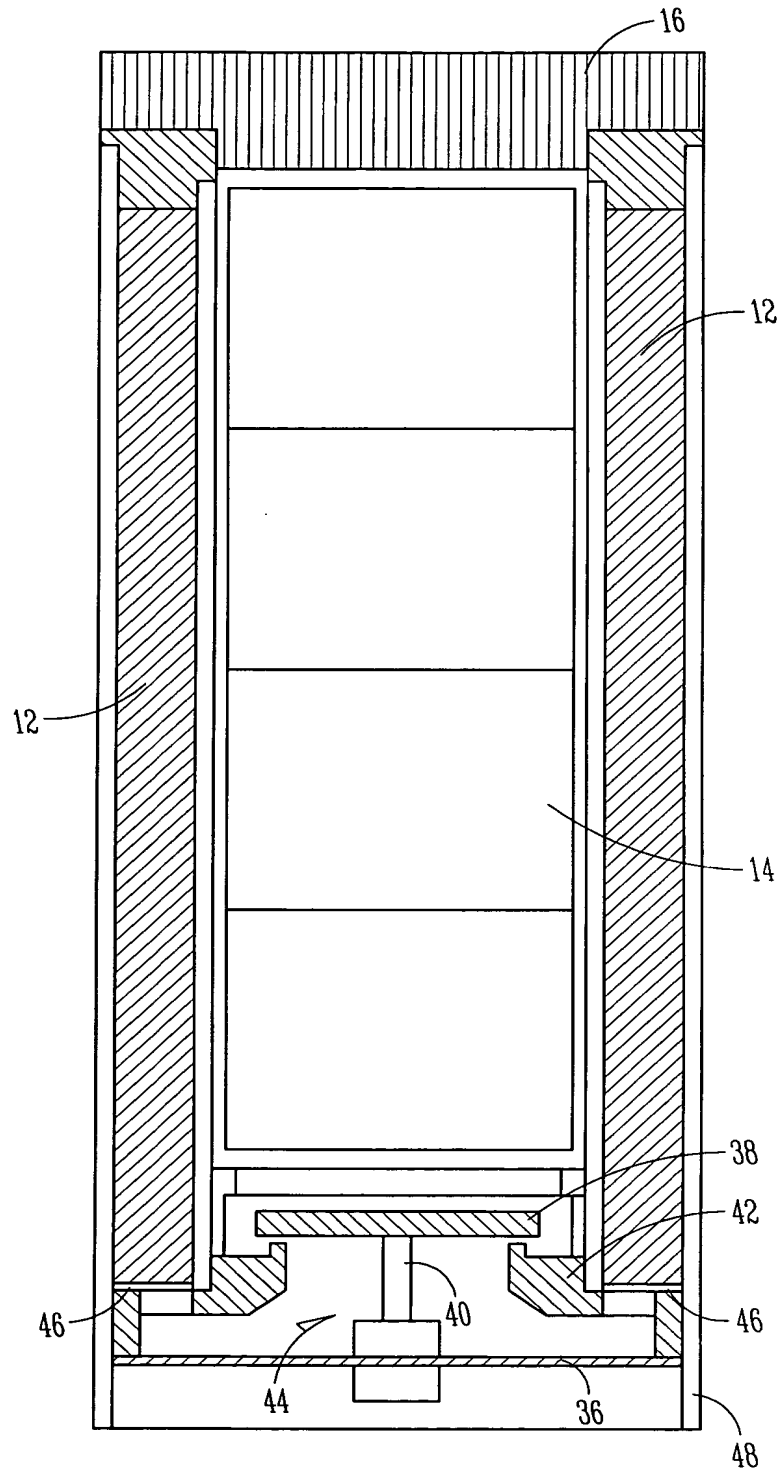


FIG. 13